WHAT IS CLAIMED IS:

1. A method of forming a simultaneous operation dual-bank flash memory device, said method comprising the steps of:

providing a plurality of flash memory arrays;

providing row and column decoders for each flash memory array; and

partitioning the plurality of flash memory arrays into a first memory bank and a second memory bank by coupling first bank row and column address lines between first bank row and column pre-decoders and the row and column decoders associated with the first memory bank, and by coupling second bank row and column address lines between second bank row and column pre-decoders and the row and column decoders associated with the second memory bank.

2. A method of forming a dual-bank flash memory device, said method comprising the steps of:

providing a plurality of flash memory arrays, each memory array having associated row and column address decoders; and

partitioning the flash memory arrays into a first memory bank and a second memory bank by:

forming first bank pre-decoded column address lines and coupling them between a first bank column address pre-decoder and the column address decoders associated with the first bank,

forming second bank pre-decoded column address lines and coupling them between a second bank column address pre-decoder and the column address decoders associated with the second bank,

forming first bank pre-decoded row address lines and coupling them between a first bank row address pre-decoder and the row address decoders associated with the first bank, and

forming second bank pre-decoded row address lines and coupling them between a second bank row address pre-decoder and the row address decoders associated with the second bank.

3. The method of claim 2, wherein the sizes of the first and second memory banks are variable, depending upon selection from and application of one a plurality of preformed metal masks used to perform the step of partitioning.

4. The method of claim 3, wherein each memory array comprises first and second halves, the first half having an associated column decoder and the second half having an associated column decoder.

5. A simultaneous operation flash memory chip having a flexible memory bank partition, comprising:

a plurality of memory arrays having associated row and column decoders, said plurality of memory arrays partitioned into first and second memory banks;

a first bank column address pre-decoder coupled to the column address decoders associated with the first memory bank;

a first bank row address pre-decoder coupled to the row address decoders associated with the first memory bank;

a second bank column address pre-decoder coupled to the column address decoders associated with the second memory bank; and

a second bank row address pre-decoder coupled to the row address decoders associated with the second memory bank.

6. The simultaneous operation flash memory chip of claim 5, wherein the partition between the first and second memory banks is determined by selecting from a plurality of preformed metal masks and applying the selected mask during manufacture of the flash memory chip.

7. The simultaneous operation flash memory chip of claim 6, wherein the plurality of metal masks are distinguished from one other by variances in pre-decoded address line patterns.

8. The simultaneous operation flash memory chip of claim 7, wherein the pattern variances determine to which memory arrays pre-decoded first bank address lines are coupled to and to which memory arrays pre-decoded second bank address lines are coupled to.

9. A simultaneous operation flash memory device having a flexible dual-bank architecture, comprising: a plurality of memory arrays capable of being partitioned into a first memory bank and a second memory bank, the partitioning of arrays within the first and second memory banks determined by how pre-decoded row and address lines are formed during a process used to fabricate the device. cl 3, 4-10

10. A method of forming a simultaneous operation flash memory device having a flexible memory bank partition, said method comprising the steps of:

providing a plurality of flash memory arrays, each memory array having associated row and column address decoders; and

partitioning the plurality of flash memory arrays into a first memory bank and a second memory bank by:

coupling first bank row and column address lines between first bank row and column pre-decoders and the row and column decoders associated with the first memory bank and

coupling second bank row and column address lines between second bank row and column pre-decoders and the row and column decoders associated with the second memory bank,

wherein the step of partitioning is performed by selecting from a plurality of preformed metal masks, said plurality of metal masks being distinguished from one other by variances in pre-decoded address line patterns.